Indian Institute of Technology Palakkad

Electrical Engineering

Research Admissions (Ph.D.)– July 2022

The candidates shortlisted for written test/interviews in the advertised areas are given below. Intimation emails will be sent on or before **May 26, 2022. Kindly note a written test followed by an interview will be conducted for all the areas except the Antennas and Electromagnetics, RF, and Microwave Integrated Circuits area. Online interviews will be conducted for candidates shortlisted for the "Antennas and Electromagnetics, RF, and Microwave Integrated Circuits" area.** The shortlisted candidates for the written test/interview will receive detailed instructions on how to proceed further.

Note 1: The candidates who will appear for the offline written test followed by interviews need to report to the IIT Palakkad (Room No: 203, Samgatha, Nila Campus) on June 09, 2022, at 08:00 am. If you clear the written test, you will be asked to appear for the interview. The interviews will be held on **June 9-10, 2022.** Hence, please be prepared to stay for two days. The candidate must confirm the attendance via email latest by **03-June-2022** (ee-admissions@iitpkd.ac.in). Your documents will be verified before the interviews**.**

Note 2: All candidates are requested to check the shortlisting criteria carefully and in case of any doubt should request a clarification from the department. The last date for contacting the department if there are any discrepancies is **02-June-2022** (ee-admissions@iitpkd.ac.in). In case a candidate who has been called feels he/she may not be satisfying the shortlisting requirements, he/she should contact the office at the earliest.

Area 1: Digital VLSI Design (PhD)

	Total	GEN	GEN-EWS	OBC-NCL	SC	ST	PwD
No of applications:	44	19	2	15	7	1	0
No of candidates shortlisted:	44	19	2	15	7	1	0
Shortlisting Criteria							
ME/MTech/MSc with overall graduation score		>= 60%	>= 54%	>= 54%	>= 40%	>= 40%	>= 40%
BE/BTech Electrical/Electronics/Instrumentation/Computer science with a valid GATE score and overall graduation score		>= 60%	>= 54%	>= 54%	>= 40%	>= 40%	>= 40%
For CFTI BE/BTech candidates with the above mentioned degrees, CGPA		>= 8	>= 7.5	>= 7.5	>=7	>=7	>= 7

LIST OF APPLICANTS SHORTLISTED FOR WRITTEN TEST

S.No.	Application No
1	PHDEEJUL2022-3965-8154
2	PHDEEJUL2022-3965-8153
3	PHDEEJUL2022-3965-8149
4	PHDEEJUL2022-3965-8118
5	PHDEEJUL2022-3965-7796
6	PHDEEJUL2022-3965-7950
7	PHDEEJUL2022-3965-8092
8	PHDEEJUL2022-3965-8067
9	PHDEEJUL2022-3965-8088
10	PHDEEJUL2022-3965-7795
11	PHDEEJUL2022-3965-6616
12	PHDEEJUL2022-3965-7884
13	PHDEEJUL2022-3965-7858
14	PHDEEJUL2022-3965-6186
15	PHDEEJUL2022-3965-7717
16	PHDEEJUL2022-3965-7776
17	PHDEEJUL2022-3965-7757
18	PHDEEJUL2022-3965-7168
19	PHDEEJUL2022-3965-7502
20	PHDEEJUL2022-3965-6831
21	PHDEEJUL2022-3965-7364
22	PHDEEJUL2022-3965-7432
23	PHDEEJUL2022-3965-7259
24	PHDEEJUL2022-3965-6763
25	PHDEEJUL2022-3965-7111
26	PHDEEJUL2022-3965-7071
27	PHDEEJUL2022-3965-7005
28	PHDEEJUL2022-3965-6969
29	PHDEEJUL2022-3965-6910
30	PHDEEJUL2022-3965-6900
31	PHDEEJUL2022-3965-6889
32	PHDEEJUL2022-3965-6713
33	PHDEEJUL2022-3965-6445
34	PHDEEJUL2022-3965-6198
35	PHDEEJUL2022-3965-6589
36	PHDEEJUL2022-3965-6625
37	PHDEEJUL2022-3965-6469
38	PHDEEJUL2022-3965-6376
39	PHDEEJUL2022-3965-6360
40	PHDEEJUL2022-3965-6177
41	PHDEEJUL2022-3965-5966
42	PHDEEJUL2022-3965-5726
43	PHDEEJUL2022-3965-5673
44	PHDEEJUL2022-3965-5640

Syllabus for written test:

A. **Digital Systems:** Introduction to Digital systems and Boolean Algebra, Basic logic operation and logic gates; Logic families -- TTL, CMOS; Combinational Logic: Decoder, encoders, multiplexers, de-multiplexers and their applications; Arithmetic circuits; Representation of signed numbers; Adders -- ripple carry, carry look ahead, BCD adders; Sequential Logic : Latches and flip flops -- SR latch, D latch, D flip-flop, JK flip-flop, T flip-flop; Setup and hold parameters; Timing analysis; Registers and counters; Shift register; Synchronous counter design using D, SR, JK flip-flops; State Machine Design : Definition of state machines; State machine as a sequential controller; Moore and Mealy state machines; Derivation of state graph and tables; Sequence detector; State table reduction using Implication table; Memory and Programmable Logic Devices : Read Only Memories, read/write memory -- SRAM/DRAM; FPGAs; Hardware description language : Modelling combinational and sequential circuits using Verilog;

B. **VLSI Design:** Basic CMOS based logic families: Static and transient behaviour of CMOS circuits, delay estimation, RC delay models, logical effort, non-ideal transistor behaviour, power dissipation, low power techniques, CMOS fabrication, CMOS based IC design, Alternate logic families, technology scaling, VLSI design styles, ASIC design flow: Front end design, synthesis, clock skew, clock jitter, static timing analysis, design for testability, physical design.

Area 2: Signal and Image Processing (PhD)

	Total	GEN	GEN-EWS	OBC-NCL	SC	ST	PwD
No of applications:	**48**	23	2	17	4	2	0
No of candidates shortlisted:	**48**	23	2	17	4	2	0
Shortlisting Criteria							
ME/MTech/MSc with overall graduation score		>= 60%	>= 54%	>= 54%	>= 40%	>= 40%	>= 40%
BE/BTech Electrical/Electronics/Instrumentation/Computer science with a valid GATE score and overall graduation score		>= 60%	>= 54%	>= 54%	>= 40%	>= 40%	>= 40%
For CFTI BE/BTech candidates with the above mentioned degrees, CGPA		>= 8	>= 7.5	>= 7.5	>=7	>=7	>= 7

LIST OF APPLICANTS SHORTLISTED FOR WRITTEN TEST

S.No.	Application No
1	PHDEEJUL2022-3965-8133
2	PHDEEJUL2022-3965-8159
3	PHDEEJUL2022-3965-8137
4	PHDEEJUL2022-3965-8135
5	PHDEEJUL2022-3965-8099
6	PHDEEJUL2022-3965-7890
7	PHDEEJUL2022-3965-7790
8	PHDEEJUL2022-3965-7112
9	PHDEEJUL2022-3965-7862
10	PHDEEJUL2022-3965-7923
11	PHDEEJUL2022-3965-7987

12	PHDEEJUL2022-3965-7858
13	PHDEEJUL2022-3965-7749
14	PHDEEJUL2022-3965-7776
15	PHDEEJUL2022-3965-7764
16	PHDEEJUL2022-3965-7168
17	PHDEEJUL2022-3965-7618
18	PHDEEJUL2022-3965-7590
19	PHDEEJUL2022-3965-6189
20	PHDEEJUL2022-3965-7491
21	PHDEEJUL2022-3965-7386
22	PHDEEJUL2022-3965-7537
23	PHDEEJUL2022-3965-6478
24	PHDEEJUL2022-3965-7502
25	PHDEEJUL2022-3965-7147
26	PHDEEJUL2022-3965-7364
27	PHDEEJUL2022-3965-7342
28	PHDEEJUL2022-3965-6414
29	PHDEEJUL2022-3965-7013
30	PHDEEJUL2022-3965-6969
31	PHDEEJUL2022-3965-5468
32	PHDEEJUL2022-3965-6572
33	PHDEEJUL2022-3965-6771
34	PHDEEJUL2022-3965-6198
35	PHDEEJUL2022-3965-6272
36	PHDEEJUL2022-3965-6373
37	PHDEEJUL2022-3965-6469

38	PHDEEJUL2022-3965-6354
39	PHDEEJUL2022-3965-6360
40	PHDEEJUL2022-3965-6351
41	PHDEEJUL2022-3965-6111
42	PHDEEJUL2022-3965-6031
43	PHDEEJUL2022-3965-5897
44	PHDEEJUL2022-3965-5798
45	PHDEEJUL2022-3965-5675
46	PHDEEJUL2022-3965-5754
47	PHDEEJUL2022-3965-5673
48	PHDEEJUL2022-3965-5602

Syllabus for written test:

PART-I Signal Processing: Sampling and reconstruction -Transform domain analysis (Fourier, and Z-transforms), -Representation of signals on orthogonal basis - Discrete systems: attributes, Z-Transform, DFT, Fast Fourier Transform algorithm, Design of FIR and IIR Digital filters; Random process: probabilistic structure of a random process; mean, autocorrelation and autocovariance functions; stationarity - strict- sense stationary and wide-sense stationary (WSS) processes: time averages and ergodicity; spectral representation of a real WSS process-power spectral density, cross-power spectral density; Linear Algebra - vector spaces, linear independence, bases and dimension, linear maps and matrices, eigenvalues, invariant subspaces, inner products, norms, orthonormal bases;

PART-II Image Processing: Image fundamentals, human visual system and image perception, Imaging geometry, Image transforms, the digitized image and its properties; Histogram Equalization and Image enhancement, Denoising, Deblurring, Spatial domain Restoration, Image Restoration in Frequency domain; Image Data Compression; Mathematical Morphology

Area 3: Antennas & Applied Electromagnetics, RF and Microwave Integrated Circuits (PhD)

Note: Online interview will be conducted for this area on 6th June 2022.

	Total	GEN	GEN-EWS	OBC-NCL	SC	ST	PwD
No of applications:	**23**	13	0	7	3	0	0
No of candidates shortlisted:	**12**	6	0	4	2	0	0
Shortlisting Criteria		B.Tech (≥75%) + M.Tech (≥ 85%) OR B.Tech (≥60%) + M.Tech (≥ 70%) + valid GATE score OR B.Tech (≥65%) + valid GATE score (≥ 300)	B.Tech (≥67.5%) + M.Tech (≥ 76.5%) OR B.Tech (≥54%) + M.Tech (≥ 63%) + valid GATE score OR B.Tech (≥58.5%) + valid GATE score (≥ 270)			B.Tech (≥50.25%) + M.Tech (≥ 59.5%) OR B.Tech (≥40.2%) + M.Tech (≥ 46.9%) + valid GATE score OR B.Tech (≥43.55%) + valid GATE score (≥ 201)	

LIST OF APPLICANTS SHORTLISTED FOR INTERVIEW (Online)

S.No.	Application No
1	PHDEEJUL2022-3965-6018
2	PHDEEJUL2022-3965-7921
3	PHDEEJUL2022-3965-7112
4	PHDEEJUL2022-3965-7674
5	PHDEEJUL2022-3965-6384
6	PHDEEJUL2022-3965-6189
7	PHDEEJUL2022-3965-7439
8	PHDEEJUL2022-3965-7013
9	PHDEEJUL2022-3965-7005
10	PHDEEJUL2022-3965-6481
11	PHDEEJUL2022-3965-5912
12	PHDEEJUL2022-3965-5685

Area 4: Control and Robotics (PhD)

	Total	GEN	GEN-EWS	OBC-NCL	SC	ST	PwD
No of applications:	**66**	27	3	27	7	2	0
No of candidates shortlisted:	**65**	27	2	27	7	2	0
Shortlisting Criteria ME/MTech/MSc with overall graduation score		>=60%	>=54%	>=54%	>=40.2 %	>=40.2%	>=40.2%
BE/BTech Electrical/Electronics/Instrumentation/Computer science with a valid GATE score and overall graduation score		>=60%	>=54%	>=54%	>=40.2 %	>=40.2%	>=40.2%

LIST OF APPLICANTS SHORTLISTED FOR THE WRITTEN TEST

Sl. No.	Application No.
1	PHDEEJUL2022-3965-8000
2	PHDEEJUL2022-3965-7790
3	PHDEEJUL2022-3965-6060
4	PHDEEJUL2022-3965-6676
5	PHDEEJUL2022-3965-6351
6	PHDEEJUL2022-3965-7641
7	PHDEEJUL2022-3965-8099
8	PHDEEJUL2022-3965-5899
9	PHDEEJUL2022-3965-7685
10	PHDEEJUL2022-3965-6530
11	PHDEEJUL2022-3965-6914
12	PHDEEJUL2022-3965-7757

13	PHDEEJUL2022-3965-7862
14	PHDEEJUL2022-3965-7518
15	PHDEEJUL2022-3965-7824
16	PHDEEJUL2022-3965-6956
17	PHDEEJUL2022-3965-7204
18	PHDEEJUL2022-3965-7838
19	PHDEEJUL2022-3965-5795
20	PHDEEJUL2022-3965-7567
21	PHDEEJUL2022-3965-5982
22	PHDEEJUL2022-3965-7623
23	PHDEEJUL2022-3965-7160
24	PHDEEJUL2022-3965-5964
25	PHDEEJUL2022-3965-5703
26	PHDEEJUL2022-3965-7884
27	PHDEEJUL2022-3965-5549
28	PHDEEJUL2022-3965-5927
29	PHDEEJUL2022-3965-7995
30	PHDEEJUL2022-3965-7475
31	PHDEEJUL2022-3965-6823
32	PHDEEJUL2022-3965-6177
33	PHDEEJUL2022-3965-7950
34	PHDEEJUL2022-3965-6750
35	PHDEEJUL2022-3965-5665
36	PHDEEJUL2022-3965-7247
37	PHDEEJUL2022-3965-7813
38	PHDEEJUL2022-3965-6881
39	PHDEEJUL2022-3965-6499
40	PHDEEJUL2022-3965-6278
41	PHDEEJUL2022-3965-7639
42	PHDEEJUL2022-3965-7213
43	PHDEEJUL2022-3965-8137

44	PHDEEJUL2022-3965-7010
45	PHDEEJUL2022-3965-6603
46	PHDEEJUL2022-3965-7618
47	PHDEEJUL2022-3965-6703
48	PHDEEJUL2022-3965-7563
49	PHDEEJUL2022-3965-6518
50	PHDEEJUL2022-3965-6936
51	PHDEEJUL2022-3965-6244
52	PHDEEJUL2022-3965-6420
53	PHDEEJUL2022-3965-7016
54	PHDEEJUL2022-3965-7590
55	PHDEEJUL2022-3965-7163
56	PHDEEJUL2022-3965-6632
57	PHDEEJUL2022-3965-7344
58	PHDEEJUL2022-3965-7923
59	PHDEEJUL2022-3965-5766
60	PHDEEJUL2022-3965-7496
61	PHDEEJUL2022-3965-6478
62	PHDEEJUL2022-3965-5652
63	PHDEEJUL2022-3965-8125
64	PHDEEJUL2022-3965-7936
65	PHDEEJUL2022-3965-6299

Syllabus for written test:

Review of Fourier and Laplace transforms, differential equations, LTI system, convolution. Introduction to control systems, Open loop, closed loop systems, Transfer function. Signal flow graph, Feedback characteristics, Negative and Regenerative feedback, Disturbances and Sensitivity reduction. Introduction to time domain Analysis, standard test signals, Transient Response, Steady-state errors, Addition of zeros, Design Specifications of higher order systems, Concept of stability, relative stability, conditions for stability, Routh-Hurwitz stability criterion, root locus, Frequency response Analysis, Bode plot, stability margins, Nyquist stability criterion, Compensators (Lead and lag compensator) design, PID controller. State space models: State Space Equations, Linearization, Solutions to Linear Time Invariant systems, Matrix Exponentials, Analysis: Equilibrium and operating points, Stability notions (BIBO, exponential, semistable, Lyapunov), Controllability, Stabilizability, Observability. Analysis on feasible operating points and tracking.

Linear Control Design: point stabilization, tracking, state feedback control - Pole placement, Lyapunov based control.

Basics of Circuit theory. RL/RC/RLC circuit analysis, OPAMPs. Basics of engineering mathematical subjects such as Linear Algebra and Partial differential equations.

Area 5: Power Electronics, Electric Drives, and Power Systems(PhD)

	Total	GEN	GEN-EWS	OBC-NCL	SC	ST	PwD
No of applications:	**89**	39	4	30	13	3	0
No of candidates shortlisted:	**89**	39	4	30	13	3	0
Shortlisting Criteria		B.Tech/BE (≥ 60%) + M.Tech (≥ 65%) OR B.Tech/BE (≥60%) + M.Tech/ME (≥ 60%) + valid GATE score OR B.Tech/BE (≥65%) + valid GATE score (≥ 250)	B.Tech/BE (≥54%) + M.Tech/ME (≥ 58.5%) OR B.Tech/BE (≥54%) + M.Tech/ME (≥ 54%) + valid GATE score OR B.Tech/BE (≥58.5%) + valid GATE score (≥ 225)	B.Tech/BE (≥40%) + M.Tech/ME (≥ 43.5%) OR B.Tech/BE (≥40%) + M.Tech/ME (≥ 40%) + valid GATE score OR B.Tech/BE (≥43.5%) + valid GATE score (≥ 167.5)			

LIST OF APPLICANTS SHORTLISTED FOR WRITTEN TEST

S. No	Application No
1	PHDEEJUL2022-3965-6513
2	PHDEEJUL2022-3965-6054
3	PHDEEJUL2022-3965-5927
4	PHDEEJUL2022-3965-5733
5	PHDEEJUL2022-3965-6299
6	PHDEEJUL2022-3965-6272
7	PHDEEJUL2022-3965-5703
8	PHDEEJUL2022-3965-8072
9	PHDEEJUL2022-3965-5964
10	PHDEEJUL2022-3965-7392

11	PHDEEJUL2022-3965-6632
12	PHDEEJUL2022-3965-7160
13	PHDEEJUL2022-3965-7623
14	PHDEEJUL2022-3965-5982
15	PHDEEJUL2022-3965-7922
16	PHDEEJUL2022-3965-6487
17	PHDEEJUL2022-3965-6122
18	PHDEEJUL2022-3965-8115
19	PHDEEJUL2022-3965-7108
20	PHDEEJUL2022-3965-7567
21	PHDEEJUL2022-3965-6420
22	PHDEEJUL2022-3965-6244
23	PHDEEJUL2022-3965-7985
24	PHDEEJUL2022-3965-6936
25	PHDEEJUL2022-3965-7838
26	PHDEEJUL2022-3965-7563
27	PHDEEJUL2022-3965-6518
28	PHDEEJUL2022-3965-8076
29	PHDEEJUL2022-3965-8148
30	PHDEEJUL2022-3965-7040
31	PHDEEJUL2022-3965-7204
32	PHDEEJUL2022-3965-6433
33	PHDEEJUL2022-3965-6619
34	PHDEEJUL2022-3965-6603
35	PHDEEJUL2022-3965-8028
36	PHDEEJUL2022-3965-5685
37	PHDEEJUL2022-3965-7951
38	PHDEEJUL2022-3965-8139
39	PHDEEJUL2022-3965-7010

40	PHDEEJUL2022-3965-7545
41	PHDEEJUL2022-3965-7926
42	PHDEEJUL2022-3965-6956
43	PHDEEJUL2022-3965-6445
44	PHDEEJUL2022-3965-7690
45	PHDEEJUL2022-3965-7936
46	PHDEEJUL2022-3965-5710
47	PHDEEJUL2022-3965-7213
48	PHDEEJUL2022-3965-8056
49	PHDEEJUL2022-3965-5553
50	PHDEEJUL2022-3965-7639
51	PHDEEJUL2022-3965-7784
52	PHDEEJUL2022-3965-6354
53	PHDEEJUL2022-3965-6499
54	PHDEEJUL2022-3965-7003
55	PHDEEJUL2022-3965-6914
56	PHDEEJUL2022-3965-6881
57	PHDEEJUL2022-3965-6653
58	PHDEEJUL2022-3965-6373
59	PHDEEJUL2022-3965-7685
60	PHDEEJUL2022-3965-5459
61	PHDEEJUL2022-3965-7439
62	PHDEEJUL2022-3965-7291
63	PHDEEJUL2022-3965-7496
64	PHDEEJUL2022-3965-7641
65	PHDEEJUL2022-3965-8145
66	PHDEEJUL2022-3965-7045
67	PHDEEJUL2022-3965-7247
68	PHDEEJUL2022-3965-7147

69	PHDEEJUL2022-3965-7344
70	PHDEEJUL2022-3965-8157
71	PHDEEJUL2022-3965-6060
72	PHDEEJUL2022-3965-5544
73	PHDEEJUL2022-3965-8050
74	PHDEEJUL2022-3965-5665
75	PHDEEJUL2022-3965-6258
76	PHDEEJUL2022-3965-7802
77	PHDEEJUL2022-3965-6750
78	PHDEEJUL2022-3965-7767
79	PHDEEJUL2022-3965-5766
80	PHDEEJUL2022-3965-7629
81	PHDEEJUL2022-3965-6511
82	PHDEEJUL2022-3965-8000
83	PHDEEJUL2022-3965-7674
84	PHDEEJUL2022-3965-6245
85	PHDEEJUL2022-3965-6823
86	PHDEEJUL2022-3965-7805
87	PHDEEJUL2022-3965-7475
88	PHDEEJUL2022-3965-7995
89	PHDEEJUL2022-3965-6508

Syllabus for written test:

Engineering Mathematics: Matrix Algebra, Systems of linear equations, Eigenvalues, Eigen vectors, Mean value theorems, Theorems of integral calculus, Evaluation of definite and improper integrals, Partial Derivatives, Maxima and minima, Multiple integrals, Fourier series, Vector identities, First order equations Higher order linear differential equations with constant coefficients, Analytic functions, Cauchy's integral theorem, Cauchy's integral, formula, Taylor series, Laurent series, Residue theorem, Solution integrals

Circuit theory: Ideal voltage and current sources, dependent sources, R, L, C, M elements; Network solution methods: KCL, KVL, Node and Mesh analysis; Network Theorems: Thevenin's, Norton's, Superposition and Maximum Power Transfer theorem; Transient response of dc and ac networks, sinusoidal steady-state analysis, resonance, two port networks, balanced three phase circuits, star-delta transformation, complex power and power factor in ac circuits.

Power systems: Basic concepts of electrical power generation, ac and dc transmission concepts, Models and performance of transmission lines and cables,Series and shunt compensation, Electric field distribution and insulators, Distribution systems, Per-unit quantities, Bus admittance matrix, Gauss- Seidel and Newton-Raphson load flow methods, Voltage and Frequency control, Power

factor correction, Symmetrical components, Symmetrical and unsymmetrical fault analysis,System stability concepts, Equal area criterion.

Control Systems: Mathematical modeling and representation of systems, Feedback principle, transfer function, Block diagrams and Signal flow graphs, Transient and Steady-state analysis of linear time invariant systems, Stability analysis using Routh-Hurwitz and Nyquist criteria, Bode plots, Root loci, Lag, Lead and Lead-Lag compensators; P, PI and PID controllers; State space model, Solution of state equations of LTI systems

Power Electronics: Static V-I characteristics and firing/gating/drive circuits for Thyristor, MOSFET, IGBT; DC to DC conversion: Buck, Boost and Buck-Boost Converters; Single and three-phase configuration of uncontrolled rectifiers; Voltage and Current commutated Thyristor based converters; Bidirectional ac to dc voltage source converters; Magnitude and Phase of line current harmonics for uncontrolled and thyristor based converters; Power factor and Distortion Factor of ac to dc converters; Single-phase and three-phase voltage and current source inverters, sinusoidal pulse width modulation.

Electrical Machines: Single phase transformer: equivalent circuit, phasor diagram, open circuit and short circuit tests, regulation and efficiency; Three-phase transformers: connections, vector groups, parallel operation; Auto-transformer, Electro-mechanical energy conversion principles; DC machines: separately excited, series and shunt, motoring and generating mode of operation and their characteristics, speed control of dc motors; Three-phase induction machines: principle of operation, types, performance, torque-speed characteristics, no-load and blocked-rotor tests, equivalent circuit, starting and speed control; Operating principle of single-phase induction motors; Synchronous machines: cylindrical and salient pole machines, performance and characteristics, regulation and parallel operation of generators, starting of synchronous motors; Types of losses and efficiency calculations of electric machines

Analog, Digital electronics and computer programming: Simple diode circuits: clipping, clamping, rectifiers; Amplifiers: biasing, equivalent circuit and frequency response; oscillators and feedback amplifiers; operational amplifiers: characteristics and applications; single stage active filters, Active Filters: Sallen Key, Butterwoth, VCOs and timers, combinatorial and sequential logic circuits, multiplexers, demultiplexers, Schmitt triggers, sample and hold circuits, A/D and D/A converters, basics of computer programming.

Area 6: Nanoelectronics, Plasmonics & Semiconductor Devices (PhD)

	Total	GEN	GEN-EWS	OBC-NCL	SC	ST	PwD
No of applications:	**64**	31	04	21	07	01	00
No of candidates shortlisted:	**40**	19	02	13	05	01	00
Shortlisting Criteria							
With min. MTech/ME cut-off of:		80%	72%	72%	53.6%		
OR							
With valid GATE score or UGC/CSIR-NET/NBHM/INSPIRE or equivalent qualification & min. MSc cut-off of:		80%	72%	72%	53.6%		
OR							
With MTech/ME/MSc & with best GATE score of atleast:		400	360	360	268		
OR							
[for Direct PhD] UG from CFTI with min. CGPA of:		8/10	7.5/10	7.5/10	7/10		

LIST OF APPLICANTS SHORTLISTED FOR WRITTEN TEST

Sl. No.	Application No
1	PHDEEJUL2022-3965-8028
2	PHDEEJUL2022-3965-6619
3	PHDEEJUL2022-3965-8092
4	PHDEEJUL2022-3965-5652
5	PHDEEJUL2022-3965-7767
6	PHDEEJUL2022-3965-6245
7	PHDEEJUL2022-3965-6900
8	PHDEEJUL2022-3965-6831
9	PHDEEJUL2022-3965-6481
10	PHDEEJUL2022-3965-6703
11	PHDEEJUL2022-3965-7795
12	PHDEEJUL2022-3965-6018
13	PHDEEJUL2022-3965-6018
14	PHDEEJUL2022-3965-6225
15	PHDEEJUL2022-3965-7392
16	PHDEEJUL2022-3965-7813
17	PHDEEJUL2022-3965-6763
18	PHDEEJUL2022-3965-7717
19	PHDEEJUL2022-3965-8135
20	PHDEEJUL2022-3965-7111
21	PHDEEJUL2022-3965-8067
22	PHDEEJUL2022-3965-7108
23	PHDEEJUL2022-3965-8145
24	PHDEEJUL2022-3965-7749
25	PHDEEJUL2022-3965-6468
26	PHDEEJUL2022-3965-7784
27	PHDEEJUL2022-3965-6530
28	PHDEEJUL2022-3965-8115
29	PHDEEJUL2022-3965-6122
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31	PHDEEJUL2022-3965-7342
32	PHDEEJUL2022-3965-6616
33	PHDEEJUL2022-3965-6713
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35	PHDEEJUL2022-3965-6111
36	PHDEEJUL2022-3965-7926
37	PHDEEJUL2022-3965-8159
38	PHDEEJUL2022-3965-7518
39	PHDEEJUL2022-3965-5897
40	PHDEEJUL2022-3965-6873

Syllabus for written test/interview:

Solid-state devices: Energy band formation; equilibrium carrier concentration, intrinsic and extrinsic semiconductors, Fermi level, Recombination and generation of carriers, carrier transport: drift and diffusion, Continuity and Poisson equation; p-n junctions; metal-oxide-semiconductor devices: MOS capacitor, MOSFET: physics and I-V characteristics; Schottky junctions. Basic Mathematics: functions, plotting etc